REMARKS

Claims 1-24 are under consideration in the application. Claims 23 and 24 stand allowed. Claims 1-6 and 12-22 stand rejected. Claims 7-11 have been objected to as being dependent upon a rejected base claim. No claims are currently amended. No new matter is added. Reconsideration and further examination of the application is respectfully requested.

The invention relates to a method of conserving power in a computer by configuring the computer, based on a measured processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded.

Rejection of claims 1, 13, 14, and 17 under 35 U.S.C. § 102(b):

Claims 1, 13, 14, and 17 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Buyuktosunoglu et al. (U.S. Pat. App. Pub. 2002/00530038) ("Buyuktosunoglu"). Applicant respectfully traverses the rejection. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1 recites in part a method comprising <u>measuring a processor load</u>. The examiner cites paragraphs [0026], [0036], and [0037] of Buyuktosunoglu as disclosing this claim element. The cited sections of Buyuktosunoglu merely describe monitoring the activity of an "issue queue" or a "storage structure" and "controlling the size of the storage structure(s) based on that measurement." The examiner makes a conclusory statement that "issue queue activity is related to processor load" (paper 20061211 page 2), but provides no evidentiary support for this claim. Applicant believes the examiner has not made out a prima facie case of anticipation with regard to the claim element of <u>measuring a processor load</u> because this claim element is not described either expressly or inherently in Buyuktosunoglu.

Buyuktosunoglu makes no mention of a processor load and does not suggest that any of its measurements are related to a processor load. At best, the examiner is asserting that a measurement of processor load is inherent in a measurement of issue queue activity. In order to for a characteristic to be inherent in a reference, it is

required that "...the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." MPEP 2112 quoting *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). "The fact that a certain result or characteristic *may* occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." MPEP 2112 citing *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (emphasis in MPEP). The examiner has not shown that measuring issue queue activity or the activity or any other storage structure must *necessarily* be a measurement of processor load.

Claim 1 further recites in part "<u>configuring the computer, based on the processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded</u>. The examiner cites paragraphs [0020], [0026], and [0027] as describing this element. However the cited passages do not support the rejection. Buyuktosunoglu does not expressly mention speculative execution, but does suggest resizing a "branch prediction table", which is a structure related to speculative execution. However, Buyuktosunoglu does not suggest that resizing the branch prediction table affects the amount of speculative execution that occurs. In fact, the method Buyuktosunoglu sizes its memory structures "depending on need or activity". (Buyuktosunoglu paragraph [0027]) In other words, Buyuktosunoglu configures its computer to accommodate the amount of an activity that is needed, not to affect the amount of the activity that occurs.

Furthermore, as Applicant has previously explained, a branch prediction table is a tool for improving the accuracy of choosing *which* code should be speculatively executed; it does not necessarily determine *whether* speculative execution is performed or not. (See Applicant's specification paragraphs [006] and [007].)

Clearly, Buyuktosunoglu does not disclose, expressly or inherently, each and every element of Applicant's claim 1, and therefore claim 1 is not anticipated by Buyuktosunoglu.

Claim 13 recites in part <u>means for measuring a processor load</u>. As is explained above with respect to claim 1, Buyuktosunoglu does not disclose this claim element.

Claim 13 further recites in part <u>means for deciding, based on the processor load, whether to enable speculative execution</u>. Nowhere does Buyuktosunoglu suggest enabling or disabling speculative execution. Changing the size of a branch prediction table, or even eliminating it, does not necessarily enable or disable speculative execution.

Clearly, Buyuktosunoglu does not disclose, expressly or inherently, each and every element of Applicant's claim 13, and therefore claim 13 is not anticipated by Buyuktosunoglu.

Claim 14 depends from claim 13 and adds further limitations, and is therefore also not anticipated by Buyuktosunoglu for at least this reason.

Claim 17 is not anticipated by Buyuktosunoglu for at least the reasons explained above with respect to claims 1 and 13.

<u>Rejection of claims 2-6, 12, and 18-22 under 35 U.S.C. § 103(a):</u>

Claims 2-6, 12, and 18-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Buyuktosunoglu in view of Atkinson (U.S. Pat. No. 5,625,826). Applicant respectfully traverses the rejection because the examiner has not made out a prima facie case of obviousness.

"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (MPEP 2143)

Without conceding either of the first two criteria, Applicant respectfully asserts that the combined references do not teach or suggest all of the limitations of the rejected claims.

Claims 2-6 and 12 depend from claim 1 and add further limitations. The examiner relies on Buyuktosunoglu to teach all of the elements of claim 1. As has been shown above, Buyuktosunoglu does not disclose all of the elements of claim 1.

Atkinson does not cure this deficiency, and the examiner's prima facie case therefore fails.

Claims 18-22 depend from claim 17 and add further limitations. The examiner relies on Buyuktosunoglu to teach all of the elements of claim 17. As has been shown above, Buyuktosunoglu does not disclose all of the elements of claim 17. Atkinson does not cure this deficiency, and the examiner's prima facie case therefore fails.
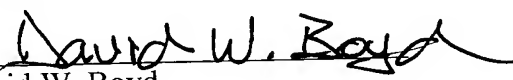
Rejection of claims 15 and 16 under 35 U.S.C. § 103(a):

Claims 15 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Buyuktosunoglu in view of Krimer et al. (U.S. Pat. App. Pub. 2004/0003215) ("Krimer"). Applicant respectfully traverses the rejection because the examiner has not made out a prima facie case of obviousness. The examiner's prima facie case is deficient for at least the reason that the combined references do not teach or suggest all of the limitations of the rejected claims.

Claims 15 and 16 depend from claim 13 and add further limitations. The examiner relies on Buyuktosunoglu to teach all of the elements of claim 13. As has been shown above, Buyuktosunoglu does not disclose all of the elements of claim 13. Krimer does not cure this deficiency, and the examiner's prima facie case therefore fails.

Applicant believes this application is in condition for allowance, and such action is earnestly solicited.

Respectfully submitted,

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